

CLAIMS:

1 1. A clock selection device adapted to select one of a pair of clock sources
2 onto an output clock line, comprising:

3 a first input clock line coupled to a first clock source;

4 a second input clock line coupled to a second clock source, the second
5 clock source asynchronous to the first clock source; and

6 a clock selection logic adapted to select from the first input clock line and
7 the second input clock line, producing an internal clock line coupled to the output
8 clock line.

1 2. The clock selection device of claim 1, the first clock source having a first
2 frequency and the second clock source having a second frequency, the second frequency
3 independent of the first frequency.

1 3. The clock selection device of claim 1, further comprising:

2 a clock synchronization logic coupled to the first input clock line, the
3 second input clock line, and the clock selection logic, adapted to synchronize the
4 first input clock line, the second input clock line, and the clock selection logic,
5 such that the internal clock line is glitch free.

1 4. The clock selection device of claim 3, the clock synchronization logic
2 comprising:

3 a first clock synchronization block, coupled to the first clock source,
4 adapted to synchronize the first clock source and the clock selection logic; and

5 a second clock synchronization block, coupled to the second clock source,
6 adapted to synchronize the second clock source and the clock selection logic.

1 5. The clock selection device of claim 4, the clock synchronization logic
2 further comprising:

3 a first clock reset signal, synchronized to the first clock signal, adapted to
4 reset the first clock synchronization block; and

5 a second clock reset signal, synchronized to the second clock signal,
6 adapted to reset the second clock synchronization block,

7 wherein the first clock reset signal and the second clock reset signal can be
8 asserted to prevent meta-stability of the clock synchronization logic.

1 6. The clock selection device of claim 3, wherein the clock synchronization
2 logic is scalable to produce a predetermined delay time between the assertion of the clock
3 select signal and the selection onto the output line by the clock selection logic.

1 7. The clock selection device of claim 1, wherein the clock selection logic
2 comprises a multiplexer with two clock input lines.

1 8. The clock selection device of claim 7, wherein the multiplexer switches
2 only when both clock input lines of the multiplexer are at the same assertion level.

1 9. The clock selection device of claim 1, further comprising:
2 a clock selection signal, asynchronous to the first clock source and the
3 second clock source, adapted to cause the clock selection logic to select one of the
4 first input clock source and the second input clock source onto the internal clock
5 line, selecting the first input clock source when the clock selection signal is
6 asserted and the second input clock source when the clock selection signal is
7 deasserted.

1 10. The clock selection device of claim 3, the clock synchronization logic
2 comprising:

3 an OR gate coupled to a clock select line and an internal feedback line of
4 the clock synchronization logic;

5 a first plurality of flip-flops coupled to the output of the OR gate and the
6 second input clock line, producing a clock switch line adapted to cause the clock
7 selection logic to switch between the first clock source and the second clock
8 source;

9 an AND gate coupled to the clock select line and the clock switch line; and

10 a second plurality of flip-flops coupled to the output of the AND gate and
11 the first input clock line, the output of the second plurality of flip-flops coupled to
12 the internal feedback line.

1 11. The clock selection device of claim 10, the clock selection logic
2 comprising:

3 an AND gate coupled to the internal feedback line and the first input clock
4 line.

1 12. The clock selection device of claim 10, the clock synchronization logic
2 further comprising:

3 an inverter coupled to the first input clock line producing an inverted first
4 input clock line coupled to the first plurality of flip-flops; and

5 an inverter coupled to the second input clock line producing an inverted
6 second input clock line coupled to the second plurality of flip-flops; and

7 the clock selection logic comprising:

8 a NAND gate coupled to the internal feedback line and the inverted first
9 input clock line.

1 13. The clock selection device of claim 1, further comprising:

2 a buffer coupled to the internal clock line, producing a buffered output
3 clock signal.

1 14. A processor-based device comprising:

2 a processor;

3 a plurality of communication controllers coupled to the processor, each of
4 the plurality of communication controllers comprising:

5 a first clock source;

6 a second clock source asynchronous to the first clock source; and

7 a clock selection device coupled to the first clock source and the
8 second clock source comprising:

9 a first input clock line coupled to the first clock source;

10 a second input clock line coupled to the second clock
11 source; and

12 a clock selection logic adapted to select from the first input
13 clock line and the second input clock line, producing an internal
14 clock line.

1 15. The clock selection device of claim 14, the first clock source having a first
2 frequency and the second clock source having a second frequency, the second frequency
3 independent of the first frequency.

1 16. The processor-based device of claim 14, the clock selection device further
2 comprising:

3 a clock synchronization logic coupled to the first input clock line, the
4 second input clock line, and the clock selection logic, adapted to synchronize the
5 first input clock line, the second input clock line, and the clock selection logic,
6 such that the internal clock line is glitch free.

1 17. The processor-based device of claim 16, the clock synchronization logic
2 comprising:

3 a first clock synchronization block, coupled to the first clock source,
4 adapted to synchronize the first clock source and the clock selection logic;

5 a second clock synchronization block, coupled to the second clock source,
6 adapted to synchronize the second clock source and the clock selection logic.

1 18. The processor-based device of claim 17, the clock synchronization logic
2 further comprising:

3 a first clock reset signal, synchronized to the first clock signal, adapted to
4 reset the first clock synchronization block; and

5 a second clock reset signal, synchronized to the second clock signal,
6 adapted to reset the second clock synchronization block,

7 wherein the first clock reset signal and the second clock reset signal can be
8 asserted to prevent meta-stability of the clock synchronization logic.

1 19. The processor-based device of claim 16, wherein the clock
2 synchronization logic is scalable to produce a predetermined delay time between the
3 assertion of the clock select signal and the selection onto the output line by the clock
4 selection logic.

1 20. The processor-based device of claim 14, wherein the clock selection logic
2 comprises a multiplexer with two input lines.

1 21. The processor-based device of claim 20, wherein the multiplexer switches
2 only when both input lines of the multiplexer are at the same assertion level.

1 22. The processor-based device of claim 14, the clock selection device further
2 comprising:

3 a clock selection signal, asynchronous to the first clock source and the
4 second clock source, adapted to cause the clock selection logic to select one of the
5 first input clock source and the second input clock source onto the internal clock
6 line, selecting the first input clock source when the clock selection signal is
7 asserted and the second input clock source when the clock selection signal is
8 unasserted.

1 23. The processor-based device of claim 22, the clock selection device further
2 comprising:

3 a clock synchronization logic coupled to the first input clock line, the
4 second input clock line, and the clock selection logic, adapted to synchronize the
5 first input clock line, the second input clock line, and the clock selection logic,
6 such that the internal clock line is glitch free.

1 24. The processor-based device of claim 23, the clock synchronization logic
2 comprising:

3 an OR gate coupled to a clock select line and an internal feedback line of
4 the clock synchronization logic;

5 a first plurality of flip-flops coupled to the output of the OR gate and the
6 second input clock line, producing a clock switch line adapted to cause the clock
7 selection logic to switch between the first clock source and the second clock
8 source;

9 an AND gate coupled to the clock select line and the clock switch line; and
10 a second plurality of flip-flops coupled to the output of the AND gate and
11 the first input clock line, the output of the second plurality of flip-flops coupled to
12 the internal feedback line.

1 25. The processor-based device of claim 24, the clock selection logic
2 comprising:

3 an AND gate coupled to the internal feedback line and the first input clock
4 line.

1 26. The processor-based device of claim 24, the clock synchronization logic
2 further comprising:

3 an inverter coupled to the first input clock line producing an inverted first
4 input clock line coupled to the first plurality of flip-flops; and

5 an inverter coupled to the second input clock line producing an inverted
6 second input clock line coupled to the second plurality of flip-flops; and

7 the clock selection logic comprising:

8 a NAND gate coupled to the internal feedback line and the inverted first
9 input clock line.

1 27. The processor-based device of claim 14, the clock selection device further
2 comprising:

3 a buffer coupled to the internal clock line, producing a buffered output
4 clock signal on the output clock line.

1 28. A method of selecting one of a pair of clock sources onto a single output
2 clock line, comprising the steps of:

3 (a) receiving a first input clock signal from a first clock source;

4 (b) receiving a second input clock signal from a second clock source,
5 the second input clock signal asynchronous to the first input clock signal; and

6 (c) connecting one of first clock signal or the second clock signal to an
7 internal clock line coupled to the output clock line.

1 29. The method of claim 28, the first clock source having a first frequency and
2 the second clock source having a second frequency, the second frequency independent of
3 the first frequency.

1 30. The method of claim 28, furthering comprising the step of:

2 buffering the internal clock line to generate the output clock line.

1 31. The method of claim 28, further comprising the steps of:
2 synchronizing the first input clock signal, the second input clock signal,
3 and step (c), such that the output clock line is glitch free.

1 32. The method of claim 31, the step of synchronizing comprising the step of:
2 delaying step (c) for a predetermined amount of time.

1 33. The method of claim 31, the step of synchronizing comprising the steps of:
2 resetting a synchronization logic with a first reset signal synchronous to
3 the first clock signal; and
4 resetting the synchronization logic with a second reset signal synchronous
5 to the second clock signal.

1 34. The method of claim 28, step (c) comprising the steps of:
2 (c1) receiving a clock select signal asynchronous to the first clock
3 signal and the second clock signal; and
4 (c2) connecting the first clock signal to the output clock line when the
5 clock select signal is asserted;
6 (c3) connecting the second clock signal to the output clock line when
7 the clock select signal is deasserted;
8 (c4) synchronizing the first input clock signal, the second input clock
9 signal, and steps (c2) and (c3), such that the output clock line is glitch free.

1 35. A clock switching mechanism with guaranteed stability, comprising:
2 a clock switching means for switching a clock source of a first clock
3 source and a second clock source to an output clock line, the second clock source
4 asynchronous to the first clock source; and
5 a clock synchronization means coupled to the first and the second clock
6 sources and the clock switching means, the clock synchronization means
7 guaranteeing the output clock line is glitch free.

1 36. The clock switching mechanism of claim 35, the clock synchronization
2 means comprising:

3 a first reset means synchronized to the first clock source for resetting the
4 clock synchronization means; and

5 a second reset means synchronized to the second clock source for resetting
6 the clock synchronization means,

7 wherein the first reset means and the second reset means can prevent meta-
8 stability of the clock synchronization means.

1 37. The clock switching mechanism of claim 35, the first clock source having
2 a first frequency and the second clock source having a second frequency, the second
3 frequency independent of the first frequency.

1 38. The clock switching mechanism of claim 35, the clock synchronization
2 means comprising:

3 a first synchronization means coupled to the first clock source for
4 synchronizing the first clock source to the clock switching means;

5 a second synchronization means coupled to the second clock source for
6 synchronizing the second clock source to the clock switching means;

7 a clock selection means coupled to the first synchronization means and the
8 second synchronization means for causing the clock switching means to switch
9 between the first clock source and the second clock source;

10 a first feedback means coupled to the clock selection means and the first
11 synchronization means for synchronizing the second synchronization means and
12 the clock selection means; and

13 a second feedback means coupled to the clock selection means and the second
14 synchronization means for synchronizing the first synchronization means
15 and the clock selection means.